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Real-Time decoding with a distributed control-stack architecture for fault-tolerant quantum computing

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Abstract

Quantum error correction (QEC) will be fundamental to ensure fault tolerance and achieve a quantum advantage. An essential element of QEC is the decoder, which protects the logical information by using the syndrome information to infer the most likely error pattern. The decoder must be accurate but also real-time to keep the quick pace of the QEC cycle (<1us for superconducting qubits). However, there are two major problems to achieve such a speed: the decoding speed per se and the communication latency with the rest of the control stack. To address the communication-latency issue, we propose and implement a distributed control-stack architecture where measurement outcomes and Pauli-frame updates are shared within a few hundreds of nanoseconds. This architecture includes and interfaces to a specialized module for running user-defined decoding algorithms. We review the most advanced proposals for decoding algorithms aimed at achieving real-time execution, with a focus on the classical computational resources (FPGA, ASIC) that are employed. This talk is aimed at researchers and experts from the quantum error correction, computer science, classical architectures and digital design communities.